ADDENDUM PAGES

Pages 2, lines 19 – 25:

The output from the amplifier 26 is input into a sample and hold circuit 28. The sample and hold circuit 28 is clocked by a first clock having a frequency f_1. The output of the sample and hold circuit 28 comprises a series of copies of the modulated signal centered about multiples of the clock frequency f_1. The output of the sample and hold circuit 28 is coupled to an oversampling delta-sigma converter 30. The delta-sigma converter 30 receives a second clock having a frequency, f_2, which is an integer multiple of the frequency f_1. In this way, the delta-sigma converter loop 30 oversamples the output signal provided by the sample and hold circuit 28; thus, after decimation filtering providing a quantized representation of the modulated signal.

Page 3, line 26 to page 4 line 13:

The inclusion of the AGC and filter circuit 24 to extend the dynamic range of a receiver is undesirable for spectrally crowded applications such as cellular communications because it makes the receiver sensitivity dependent upon signals and interference that are outside the signal channel. For example, it is possible for a strong signal in an adjacent channel to capture the receiver front end and desensitize the receiver so that a weak signal in the channel of interest is undetectable. In order to avoid this type of operation, the AGC and filter circuit 24 must be capable of rejecting the out-of-band signals before they desensitize the receiver. The resultant filter included in the AGC and filter circuit 24 is typically a tunable narrowband, bandpass filter. Because it is currently not practical to realize such a filter on a semiconductor substrate, inclusion of such a filter significantly increases the cost and complexity of the receiver. Thus, although the AGC portion and LNA portions can be implemented on a high frequency semiconductor substrate, the design requires the signal path to exit the semiconductor for filtering. In order to exit the semiconductor, the signal levels must be increased thereby increasing the size, cost and power consumption of the receiver. In addition, the filter itself is typically implemented using [of] discrete analog components, further increasing the size and cost of the receiver. Finally, the inclusion of automatic gain control creates a DC offset error which is a function of the automatic gain control setting, making offset correction difficult to implement.

Page 4, line 28 to page 5, line 4:

In one embodiment, inversion is performed by producing an inverted signal representation of the incoming waveform, producing [an]a non-inverted signal representation of the incoming waveform, coupling the inverted signal representation to a first input port of a switch, coupling the non-inverted signal representation to a second input port of the switch, and coupling the conversion clock to a control port of the switch, wherein the incoming waveform is received over an antenna and wherein an amplitude of the incoming waveform is in fixed proportion to an amplitude of a signal strength received by the antenna.